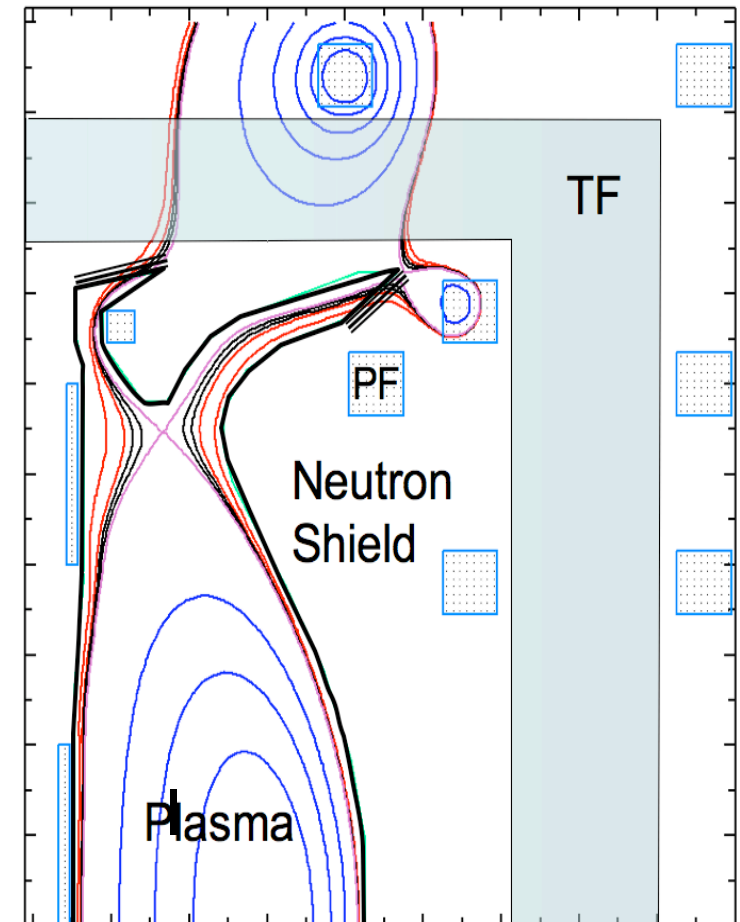


Super-X Divertor helps enable the full potential of ST

- Integrated operation of ST is challenging because of higher power density of ST
 - ST: high power density AND simultaneous high core τ_E , high core β , high neutron fluence
 - SXD addresses this, enabling full ST potential
- SXD uniquely expands the divertor plate to larger R_{major} to increase wetted area, line length:
 - SXD most beneficial for low aspect ratio
 - Largest relative increase in R_{major} , wetted area
 - Enables $2\text{-}3 \times P_{\text{SOL}}$ than other novel divertor geometries (snowflake, old XD, plate tilt,..)
 - SXD allows largest increase in line length-addresses the short line length of ST divertor
 - lowers divertor plate temperature
 - reduces high Z plasma impurities (& accumulation)
 - Increases divertor radiation
 - Largest synergisms with liquid metals
 - MHD problems \sim local B^2 smallest in SXD
 - Longest radial trunk \Rightarrow mitigates evaporation



Integrated Operation: SXD impacts other goals

- Greatly reduces the core radiation requirements to save divertor
 - Improves core confinement
 - More power through pedestal => higher pedestal =>
 - Better core confinement
 - Broader pressure profiles => higher beta
- Allows lower edge density & recycling => higher confinement?
 - Divertor is the limiting factor- SXD increases wetted area, line length
 - Lower edge density => greater CD efficiency, higher bootstrap current => higher beta
 - Lower edge density => lower v_* , η => likely higher confinement?
 - Longer line length allows low plate plasma temperature
 - Less high Z sputtering => less high Z accumulation => higher confinement
- Improved prospects for liquid metal operation
 - Order of magnitude reduction in liquid MHD; also evaporation mitigation
- Reduces neutron damage
 - Enables use of ITER divertor plate hardware for CTF with minimum of:
 - Additional R&D time, money
 - Risk
 - Availability loss from frequent replacement, failure, etc.
 - (Since ITER hardware degrades after ~ 1 dpa, much less than CTF goal)

Divertor limits power density

- In steady state operation, the divertor limits the attainable power density even on ITER

2007 ITER Physics Basis:

“The fusion gain in steady state maximizes at low density for constant β_N . The limitation on reducing the density in next generation tokamaks is set by the impact on the divertor.”

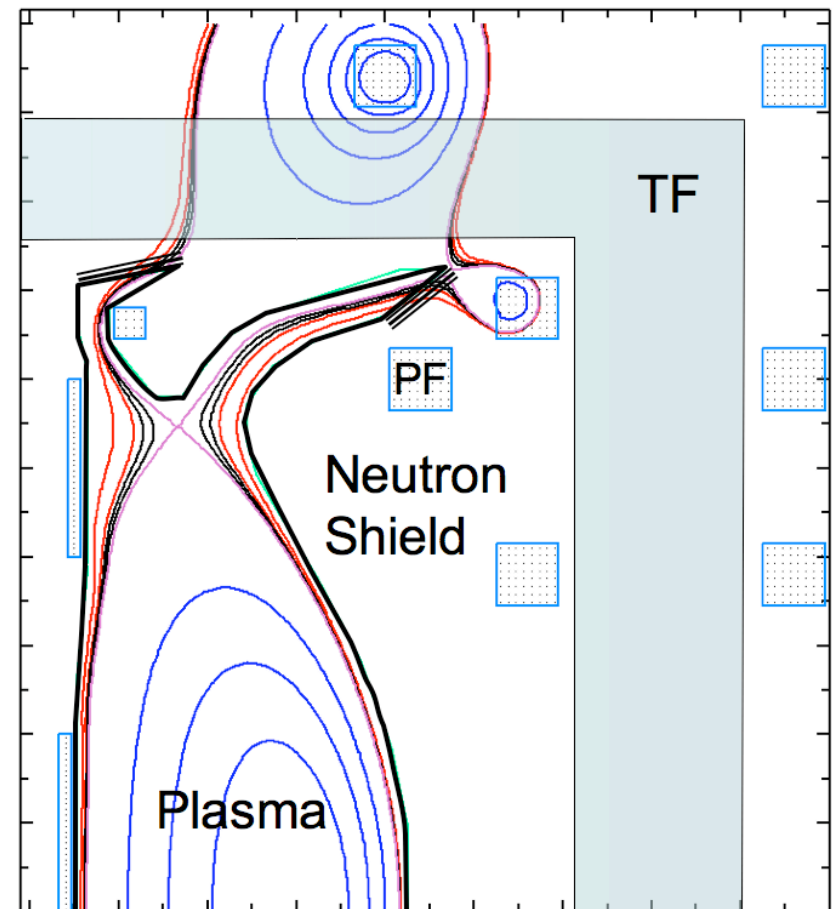
“It should be noted that presently developed advanced scenarios have not yet provided fully integrated scenarios and several issues remain to be solved, such as edge compatibility with the divertor”

- Novel divertors are an important facet of ST research to ensure the ST can reach its maximum potential power density
 - ST can also act as a testbed for divertor development for normal aspect ratio AT modes

1 deg limit => SXD is the *only* way to increase A_w

$$A_w = \frac{B_{p,sol}}{B_{div}} \frac{A_{sol}}{\sin(\theta)} \approx \left[\frac{B_p}{B_t} \right]_{sol} \frac{R_{div}}{R_{sol}} \frac{A_{sol}}{\sin(\theta)}$$

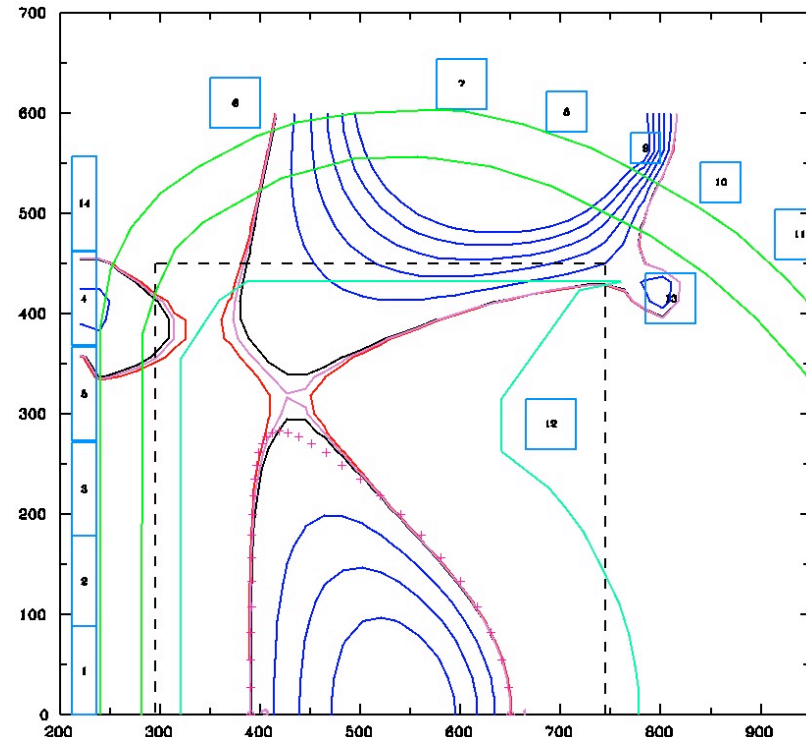
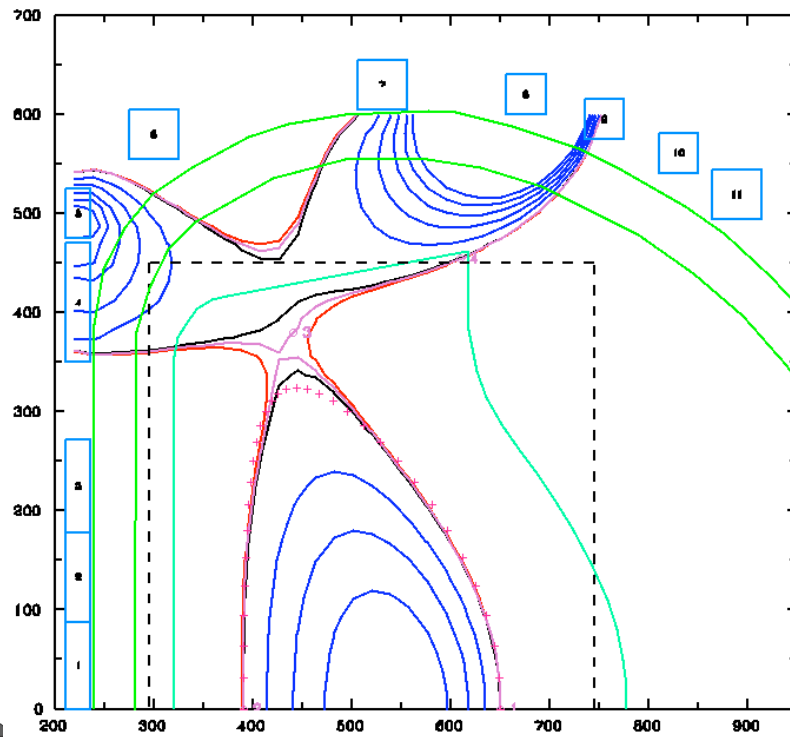
- Angle between total B and plate *must be* more than 1 degree, so
- Flux expansion gains via any route (tilting plate, XD, snowflake--) are **equally** limited
- SOL width (so A_{sol}) is a given by upstream physics
- So *only* knob left is R_{div}/R_{sol} --- maximization of which is a crucial SXD strategy. Direct gain of ~ 2 in A_w



HPDX - CORSICA Equilibrium

SXD for Superconducting ARIES-AT Reactor

- SXD has been implemented **within existing TF coils** of SC reactors:
 1. Either with all axisymmetric PF coils outside TF coils (left fig.), or
 2. Or with modular coils not linked with TF coils (right fig.)
- No extra TF “real estate” is needed even for existing reactor designs
- The net MA-m in PF coils and their locations are similar to the standard divertor case



Example: SXD can save NHTX from heat flux menace

- With SXD & 30 MW, peak heat flux can be kept under 10 MW/m²
- Not possible with standard divertor (peak stays at 30-40 MW/m²)
- SOLPS 2-D calculations (Canik & Maingi) confirm 1-D code expectations

